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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,260	10/03/2003	Masahiro Tanaka	243492US2S	8734
22850	7590	12/22/2004	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			NGUYEN, THINH T	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/677,260	Applicant(s) TANAKA ET AL.	
	Examiner Thinh T Nguyen	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☒ Claim(s) 6-10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 03 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED OFFICE ACTION**

1. Applicant election of claims 1-10 without traverse for prosecution of the present Application in the communication with the Office on 10/30/2004 is acknowledged.

#### **Specification**

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

#### **Drawings**

3. Fig. 20 and 21 are not designated by a legend such as "prior art". The legend is necessary in order to clarify what applicant's invention is (see MPEP paragraph 608.02).

#### **Claim Rejections - 35 USC § 102**

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent,

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except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant

Admitted Prior Art (the AAPA) disclosed in fig 20 and fig 21.

#### REGARDING CLAIM 1

The AAPA discloses (fig 20, fig 21, paragraph [0008] to [0011]) a power semiconductor device comprising: a semiconductor active layer (fig 21 layer 101); a first base layer (fig 21 layer 101) of a first conductivity type disposed in the active layer; a plurality of trenches disposed in a surface of the active layer at intervals to partition a main cell and a dummy cell (fig 20), and to reach the first base layer; a collector layer (fig 21 layer 103) of a second conductivity type disposed on the first base layer, at a position remote from the trenches; a second base layer (fig 21 layer 107) of the second conductivity type disposed in the main cell and on the first base layer; an emitter layer (fig 21 layer 108) of the first conductivity type disposed on the second base layer; a buffer layer of the second conductivity type (fig 21 layer 109) disposed in the dummy cell and on the first base layer; a gate electrode (fig 21 layer 106) disposed in each trench to face, through a gate insulating film (fig 21 layer 105), a portion of the second base layer sandwiched between the first base layer and the emitter layer; a collector electrode (fig 21 layer 111) disposed on the collector layer; an emitter electrode (fig 21 layer 112) disposed on the second base layer and the emitter layer; and a partition structure (fig 20, fig 21) disposed in the surface of the active layer to electrically isolate the buffer layer from the emitter electrode.

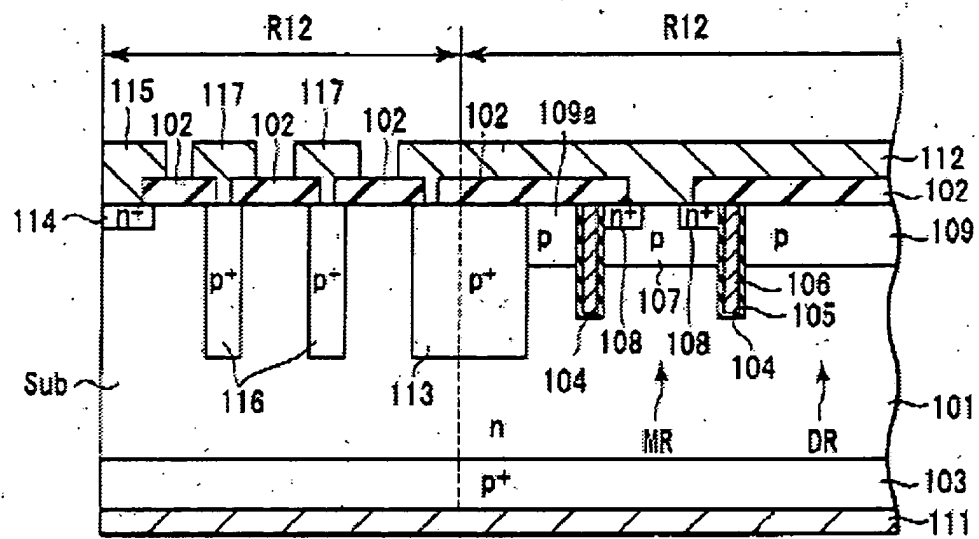
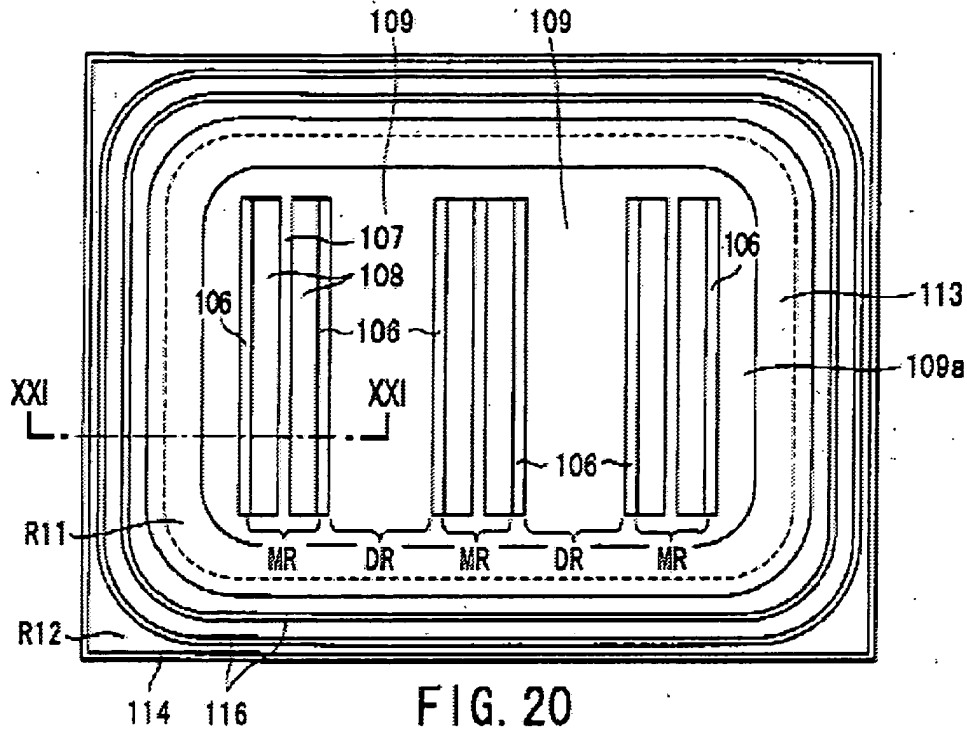


FIG. 21



REGARDING CLAIM 2

The AAPA ( fig 20,fig 21) discloses a power semiconductor device wherein the partition structure that comprises: a partition wall ( fig 21 layer 105) formed of a partition trench disposed in the surface of the active layer.

REGARDING CLAIM 3

The AAPA (fig 20,fig 21) discloses a power semiconductor device wherein the partition trench has a depth substantially the same as the trenches.

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**REGARDING CLAIM 4**

The AAPA (fig 20,fig 21) discloses a power semiconductor device wherein a conductive layer (fig 21 layer 106) is disposed in the partition trench and wrapped in an insulating film and wherein the conductive layer is electrically connected to the gate electrode paragraph [0009] line 6.

**REGARDING CLAIM 5**

The AAPA (fig 20,fig 21) discloses a power semiconductor device wherein the partition trench is filled with an insulating layer (fig 21 layer 105).

**ALLOWABLE SUBJECT MATTER**

6. Claims 6, 7 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim.

Claim 6,7 are considered allowable since the prior fails to teach a structure of a power semiconductor wherein the partition structure comprises a partition wall formed of a partition layer of the first conductivity type disposed in the surface of the active layer.

7. Claims 8 is objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim.

Claim 8 is considered allowable since the prior fails to teach a structure of a power semiconductor wherein the partition structure comprises a partition wall formed of a combination of a partition trench and a partition layer of the first conductivity type,

8. Claims 9 is objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim.

Claim 9 is considered allowable since the prior fails to teach a structure of a power semiconductor wherein the partition structure comprises dummy cell end walls, which bridge ends of the trenches one on either end of the dummy cell and cooperate with the trenches to surround the dummy cell.

9. Claims 10 is objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim.

Claim 10 is considered allowable since the prior fails to teach a structure of a power semiconductor wherein the partition structure comprises main cell end walls, which bridge ends of the trenches one on either end of the main cell and cooperate with the trenches to surround the main cell.



10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

12. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

### CONCLUSION

13. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Himi et al. (US patent 5,525,824) disclose a semiconductor device with isolation regions.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

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The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen



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MICHAEL TRAN  
PRIMARY EXAMINER